IN THE CLAIMS:

Please note that all claims currently pending and under consideration in the referenced application are shown below. The listing of claims will replace all prior versions and listings of claims in the application.

Please amend claims 1, 12 and 36 as set forth below.

Listing of Claims:

1. (Currently Amended) A method of fabricating an integrated circuit package comprising:

providing a semiconductor die having a plurality of bond pads on an active surface thereof;

providing a lead frame including a plurality of conductive leads;

electrically coupling a first bond pad of the plurality of bond pads to a first portion of at least one conductive lead of the plurality of conductive leads;

electrically coupling a second bond pad of the plurality of bond pads to a second portion of the at least one conductive lead; ~~and~~

electrically isolating the first portion of the at least one conductive lead from the second portion of the at least one conductive lead; and

disposing a volume of electrically insulating material between the first portion of the at least one conductive lead and the second portion of the at least one conductive lead subsequent the electrically isolating the first portion from the second portion.

2. (Original) The method of claim 1, further comprising encapsulating the semiconductor die and at least a portion of the lead frame in a dielectric material.

3. (Original) The method of claim 2, wherein the electrically isolating the first portion from the second portion is effected subsequent to the encapsulating.

4. (Original) The method of claim 1, wherein the electrically isolating the first portion from the second portion of the at least one conductive lead includes mechanically severing the at least one conductive lead between the first portion and the second portion.

5. (Original) The method of claim 1, wherein the electrically isolating the first portion from the second portion of the at least one conductive lead includes etching to sever the at least one conductive lead between the first portion and the second portion.

6. (Original) The method of claim 1, wherein the electrically coupling the first bond pad to a first portion of the at least one conductive lead includes wire bonding.

7. (Previously Presented) The method of claim 6, wherein the electrically coupling the second bond pad to the second portion of the at least one conductive lead includes wire bonding.

8. (Original) The method of claim 1, further comprising forming a notched region in a surface of the at least one conductive lead between the first portion and the second portion.

9. (Original) The method of claim 8, further comprising encapsulating the semiconductor die and at least a portion of the lead frame including the notched region of the at least one conductive lead in a dielectric material.

10. (Original) The method of claim 9, wherein the electrically isolating the first portion from the second portion includes separating the first portion from the second portion while leaving at least some dielectric material in the notched region.

11. (Original) The method of claim 10, wherein the separating the first portion from the second portion includes cutting the at least one conductive lead into the notched region from an opposing surface of the at least one conductive lead.

12. (Currently Amended) A method of forming an array of electrically conductive elements on an integrated circuit package, the method comprising:

securing a semiconductor die having a plurality of bond pads on an active surface thereof to a lead frame having a plurality of leads;

electrically coupling at least two spaced locations of each lead of the plurality of leads ~~at spaced locations~~ with ~~one of~~ at least two different bond pads of the plurality of bond pads; ~~and~~

severing each lead between the at least two spaced locations to form at least two electrically isolated conductive elements; and

disposing an electrically insulative material between the at least two spaced locations of each lead subsequent the severing.

13-35 Canceled

36. (Currently Amended) A method of fabricating a semiconductor die assembly, comprising:

placing a semiconductor die within a plurality of leads extending laterally outwardly from peripheral edges thereof;

wire bonding bond pads on the semiconductor die to spaced locations on each of the leads of the plurality;

transfer molding a dielectric encapsulant over the semiconductor die, wire bonds and the plurality of leads, leaving undersurfaces of the plurality of leads exposed; ~~and~~

severing each of the plurality of leads between the spaced locations; and

disposing a volume of electrically insulative material between the spaced locations subsequent severing each of the plurality of leads.

37. (Original) The method of claim 36, further comprising notching upper surfaces of the leads between the spaced locations before the placing the semiconductor die within the plurality of leads.

38. (Original) The method of claim 36, wherein the placing the semiconductor die includes securing the semiconductor die to a die paddle located within the plurality of leads.

39. (Original) The method of claim 36, wherein the severing is effected by making a linear cut between the spaced locations on each lead extending from a common peripheral edge.

40. (Previously Presented) The method of claim 39, further comprising notching upper surfaces of the leads between the spaced locations before the placing the semiconductor die within the plurality of leads, and wherein the linear cut is extended substantially only to a depth sufficient to intersect bottoms of the notches so that some dielectric encapsulant remains between the spaced locations.

41-44 Canceled

Please enter new claims 45 through 48 as set forth below.

45. (New) The method according to claim 1, wherein providing a lead frame including a plurality of conductive leads further includes providing the lead with a die paddle and arranging each of the plurality of conductive leads so as to extend away from an adjacent peripheral edge of the die paddle at an acute angle relative thereto.

46. (New) The method according to claim 12, wherein securing a semiconductor die to a leadframe further includes providing the lead frame with a die paddle and arranging each of the plurality of conductive leads so as to extend away from an adjacent peripheral edge of the die paddle at an acute angle relative thereto.

47. (New) The method according to claim 36, wherein placing a semiconductor die within a plurality of leads further includes providing a lead frame having a die paddle and arranging each of the plurality of conductive leads so as to extend away from an adjacent peripheral edge of the semiconductor die at an acute angle relative thereto.

48. (New) The method according to claim 37, wherein notching upper surfaces of the leads further comprises defining a concavity within each of the plurality of leads exhibiting a width taken in a direction extending between the spaced locations of a first distance and wherein severing each of the plurality of leads between the spaced locations further includes separating the spaced locations by a second distance less than the first distance.